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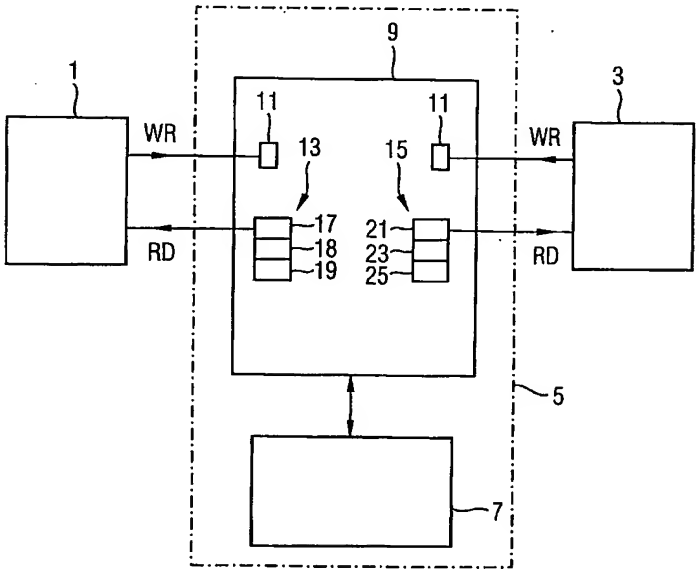
(54) Title: MAILBOX INTERFACE BETWEEN PROCESSORS



(57) Abstract: A mailbox (5) is proposed for transferring data between two processors (1, 3). The mailbox (5) includes a main memory (7) and an ancillary memory (13, 15). The mailbox stores received data packets in the main memory (7), and stores in the ancillary memory (13, 15) those data packets which are to be read out soonest. In response to a read signal, the mailbox (5) transmits data from the ancillary memory (13, 15) and replenishes the ancillary memory (7) by transferring data to it from the main memory (7). This means that the mailbox (5) can transmit data on the clock cycle following reception of the read signal.

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MAILBOX INTERFACE BETWEEN PROCESSORS

Field of the invention

The present invention relates to a mailbox interface between two data processors.

Background of Invention

It is known to transfer data between two processors using a mailbox in which data to be transferred is stored temporarily. Fig. 1 shows a typical such arrangement in which data is transferred between processors 1, 3, which may be respectively a MIPS processor (which is the name of a processor sold by MIPS Technology, Inc) and an OAK DSP (which is the name of a digital signal processor sold by DSP Group Inc.).

The process operates using a mailbox 5 which includes a shared memory 7 and a control unit 9. The mailbox 5 receives messages to be transferred between the two processors and made up of a plurality of data packets. For example, in the case of a message to be sent from the processor 1 to the processor 3, the message is transmitted as a sequence of one or more write instruction data packets (WR) from the processor 1 to the control unit 9, which stores the packets in the shared memory 7. When the message has been fully transmitted to the shared memory 7 an interrupt signal is transmitted to the processor 3, which transmits read command to the control logic 9. In response to the read command the control unit 9 reads stored data packets (RD) from the memory 7, and transmits them to the processor 3. An identical operation is performed in reverse if the processor 3 wants to transmit a message to the processor 1: the processor 3 sends a plurality of write messages (WR) to the control unit 9, then an interrupt signal to the processor

1, which responds by sending read command to the control unit 9, which sends the data in packets (RD) to the processor 1.

Consider this operation in more detail. During the write operation, the control unit 9 receives from the processor 1, in the same clock cycle, a write command, an address signal (indicating the address of processor 1), and the data. The control unit conventionally copies the data to a write register 11 corresponding to the processor 1, from where the data is transferred to the memory 7 on the next clock cycle. Thus, as far as the processor 1 is concerned, the data packet is transferred to the mailbox in a single clock cycle, although the data only reaches the memory 7 after two clock cycles.

By contrast, the read operation cannot be performed as quickly. In a first clock cycle the control unit 9 receives a read signal from the processor 3 (including the read command and the address of the processor 3). Reading the respective packet from the memory 7 generally takes the control unit 9 at least two clock cycles. The first cycle is used to set ("manipulate") the pointer which determines which location in the memory 7 data is read from, and to set-up the address within the shared memory, and the second cycle is used to latch in the data from the shared memory. Thus the processor 3 only receives the data at least three clock cycles after the read command is transmitted. Furthermore, it is difficult to arrange the pointer manipulation and address set-up to be performed in a single cycle when the reading processor is a MIPS processor which typically operates at a speed of 150 MHz. In the case of the OAK processor it is difficult to meet this timing because the two-phase clock used in the OAK design.

Since there is a delay of several cycles between one of the processors 1, 3 transmitting a read signal and actually receiving the data from the mailbox, the processor receiving the message must employ wait states in which it waits a

number of clock cycles for the data to reach it. This slows down the operation of that processor.

Summary of the Invention

The present invention aims to provide a new and useful method of operating a data mailbox, and a data processing system which employs the method.

In general terms, the method proposes that the mailbox for temporary storing data packets includes a main memory and an ancillary memory. The mailbox stores received data packets in the main memory, and stores in the ancillary memory those data packets which are to be read out soonest. In response to a read signal, the mailbox transmits data from the ancillary memory, and replenishes the ancillary memory by transferring data to it from the main memory.

The ancillary memory is typically implemented as registers, which means that data can be read out of it immediately (on the next clock cycle), rather than after a delay of one or more clock cycles. Thus, the present invention makes it possible to achieve a read back after zero wait states. Accordingly the data transfer rate is increased between the mailbox and the processor, and the computational power of the processor(s) is not wasted in wait states.

The operation of transmitting data from the ancillary memory may be performed in parallel with (on the same clock cycle as) the replenish operation, so that the ancillary memory does not run out of data irrespective of the number of consecutive read operations.

Conveniently, the ancillary memory may be a FIFO memory.

The main memory of the mailbox may be implemented as in conventional systems, that is such that more than one clock periods are required to extract data from a location in the main memory to which the pointer is not already pointing. The ancillary memory is preferably capable of storing an amount of data which is at least equal to the data to be transmitted during this time. Thus, the ancillary memory is preferably arranged to store at least the number of data packets which are transferred during three clock cycles.

Preferably, a respective ancillary memory is provided for each of the locations (processors) to which the mailbox writes data, each ancillary memory storing the data which is next to be transmitted to that location.

Brief Description of The Figures

Preferred features of the invention will now be described, for the sake of illustration only, with reference to the following figures in which:

Fig. 1 shows schematically a known memory;

Fig. 2 shows schematically an embodiment of the present invention; and

Fig. 3 shows the process of transferring data from the mailbox a processor in the embodiment of the invention.

Detailed Description of the embodiments

Referring to Fig. 2, data processing system which is an embodiment of the invention is shown. Many elements of Fig. 2 correspond to those of Fig. 1 and are given the same reference numerals. The implementation of features shared between the embodiment and the conventional system of Fig. 1 may be as in the conventional system.

As shown the embodiment includes a number of processors 1, 3. For simplicity only two processors are shown, but the invention is not limited in this respect.

The mailbox 9 of the embodiment includes, in addition to the main memory 7, two ancillary memories 13, 15 located within the control unit. The ancillary memory 13 is a FIFO memory made up of three registers 17, 18, 19, and is used for transmitting data from the main memory 7 to the processor 1 as described below. The ancillary memory 15 is equivalent in construction to the ancillary memory 13. Specifically, the ancillary memory 15 is a FIFO memory made up of three registers 21, 23, 25, and is used for transmitting data from the main memory 7 to the processor 3 as described below.

Consider the operation of transferring a message including a plurality of data packets from the processor 1 to the processor 3. The data packets are received from the processor 1 by the control unit 9 on successive data cycles and written to the write register 11. The write register transfers the data packets to the memory 7 in the manner described above in relation to the known device. The control unit 9 then reads back from the memory 7 in order the first three data packets which are to be transmitted to the processor 3, and writes them in order to the memory 15. Since the memory 15 is a FIFO memory, this means that the first data packet is stored in register 21, the second data packet is stored in the register 23 and the third data packet is stored in the register 25.

Note that in an alternative embodiment, the write register may write the first three data packets of the message in order directly to the ancillary memory 15, and write the rest of the data packets in the message into the memory 7.

In either case, a pointer is maintained pointing to the address in the memory 7 of the fourth packet in the message.

The sequence of operations in which data is sent to the processor 3 is shown in Fig. 3, where time is shown advancing from the top of the diagram to the bottom, and the clock signals are shown as dashed lines.

In a first clock period (clock period "0"), the processor 3 transmits a read signal to control unit 9, in response to the interrupt signal from the processor 1.

In the next clock period (clock period "1"), the control unit 9 transmits the output of the ancillary memory 15 (i.e. the data in the register 21) to the processor 3. The data in the register 23 is thus transferred to the register 21, and the data in the register 25 is transferred to the register 23. In the same clock cycle, the control unit 9 uses the pointer to extract from the memory 7 the fourth data packet which is to be transmitted to the processor 3. The control unit 9 writes this fourth data packet to the ancillary memory 15, so that it is written to the register 25.

Furthermore, during clock period "1", the processor sends a read signal to the mailbox.

In response to the read signal transmitted in clock period "1", in the next clock period (clock period "2") the control unit transmits the new output of the ancillary memory 15 to the processor 3. The data in the register 23 is transferred to the register 21, and the data in the register 25 is transferred to the register 23. The control unit 9 again replenishes the register 25 by extracting the fifth data packet which is to be transmitted to the processor 3, and writes it to the ancillary memory 15, so that it is written to the register 25.

This process continues until all data packets have been transferred to the processor 3.

The operation of sending data packets from the processor 3 to the processor 1 is exactly as described above, but with the ancillary memory 13 used in place of the ancillary memory 15.

Typically, the mailbox 5 is implemented as a single integrated circuit device. The device can be located within a data processing system which further includes the processors 1, 3, and the data is transferred between the mailbox 5 and the processors 1, 3 using a bus of the data processing system according to conventional methods.

Although only a single embodiment of the invention has been described, the invention is not limited in this respect and many variations are possible within the scope of the invention as will be clear to a skilled reader.

For example, it is possible to adapt the mailbox for use in an arrangement with more than two processors. In such a case, a FIFO ancillary memory is preferably provided for each of the processors, to store the first few data packets of any messages which are sent to that processor.

Note that if multiple messages are sent to a given processor, the corresponding ancillary memory stores the first few data packets of the first of these messages which the ancillary memory receives. When all the packets of this message have been successively written to the FIFO ancillary memory (i.e. as earlier packets of the message are successively read by the processor to which the message is directed), further read instructions from the processor cause the FIFO ancillary memory to be replenished successively using respective data packets of the second message.

Claims

1. A mailbox for temporally storing messages which include a sequence of one or more data packets and which are being transferred between a plurality of locations, the mailbox including a main memory, an ancillary memory, and a control unit which is arranged:

to receive the messages from one of the locations,

to store at least the first data packet of the message in the ancillary memory and other data packets of the message in the main memory, and

in response to a read signal, to transmit a data packet from the ancillary memory to another location, and to replenish the ancillary memory by transferring a data packet to it from the main memory.

2. A mailbox according to claim 1 in which the ancillary memory is a FIFO memory implemented as registers.

3. A mailbox according to claim 1 in which the operation of transmitting the data packet from the ancillary memory is performed on the same clock cycle as the replenish operation.

4. A mailbox according to claim 1, claim 2 or claim 3 in which the ancillary memory stores a number of data packets which is at least equal to the number of clock periods required by the mailbox to extract any data packet from the main memory.

5. A mailbox according to any preceding claim including a plurality of ancillary memories, different ones of the ancillary memories being arranged to store data being transferred to different locations.

6. A data processing system including a plurality of processors and a mailbox according to any preceding claim 1, a first of the processors being

arranged to transfer a message to the second processor by transmitting it as a series of data packets to the mailbox and sending a signal to the second processor to indicate the presence of the message in the mailbox, the second processor being arranged in response to send a read signal to the mailbox.

7. A method for temporally storing messages which include a sequence of one or more data packets and which are being transferred between a plurality of locations, the method including:

receiving the messages from one of the locations,

storing at least the first data packet of the message in the ancillary memory, and one or more other data packets of the message in the memory, and

in response to a read signal, transmitting data from the ancillary memory to another location, and replenishing the ancillary memory by transferring data to it from the main memory.

8. A method for transferring a message between two processors using a mailbox having a main memory and an ancillary memory, the method including:

a first of the processors transmitting the message to a mailbox as a sequence of one or more data packets, and sending an interrupt signal to a second of the processors;

the mailbox receiving the data packets, storing at least the first data packet of the message in the ancillary memory, and other data packets of the message in the main memory,

the second of the processors in response to the interrupt signal sending a read signal to the mailbox, and

the mailbox in response to a read signal, transmitting data from the ancillary memory to second processor, and replenishing the ancillary memory by transferring data to it from the main memory.

FIG 1

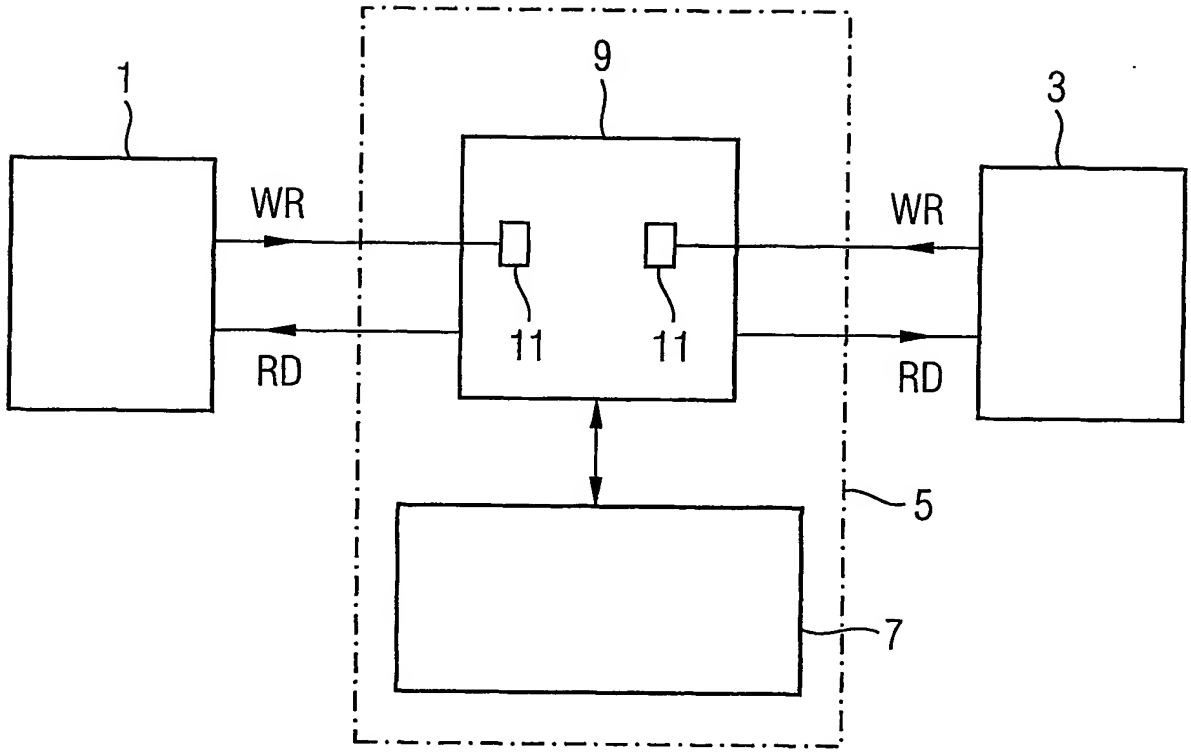


FIG 2

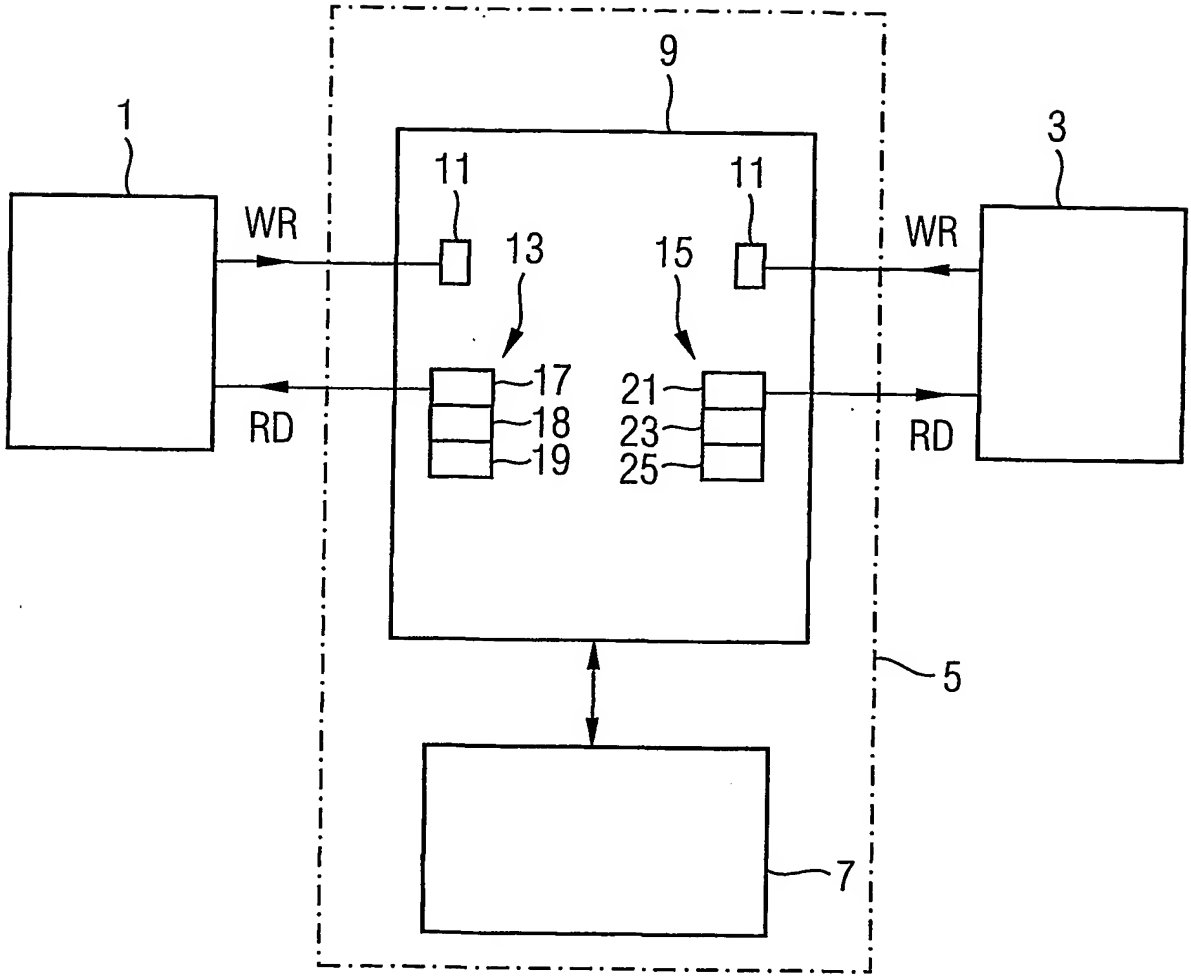
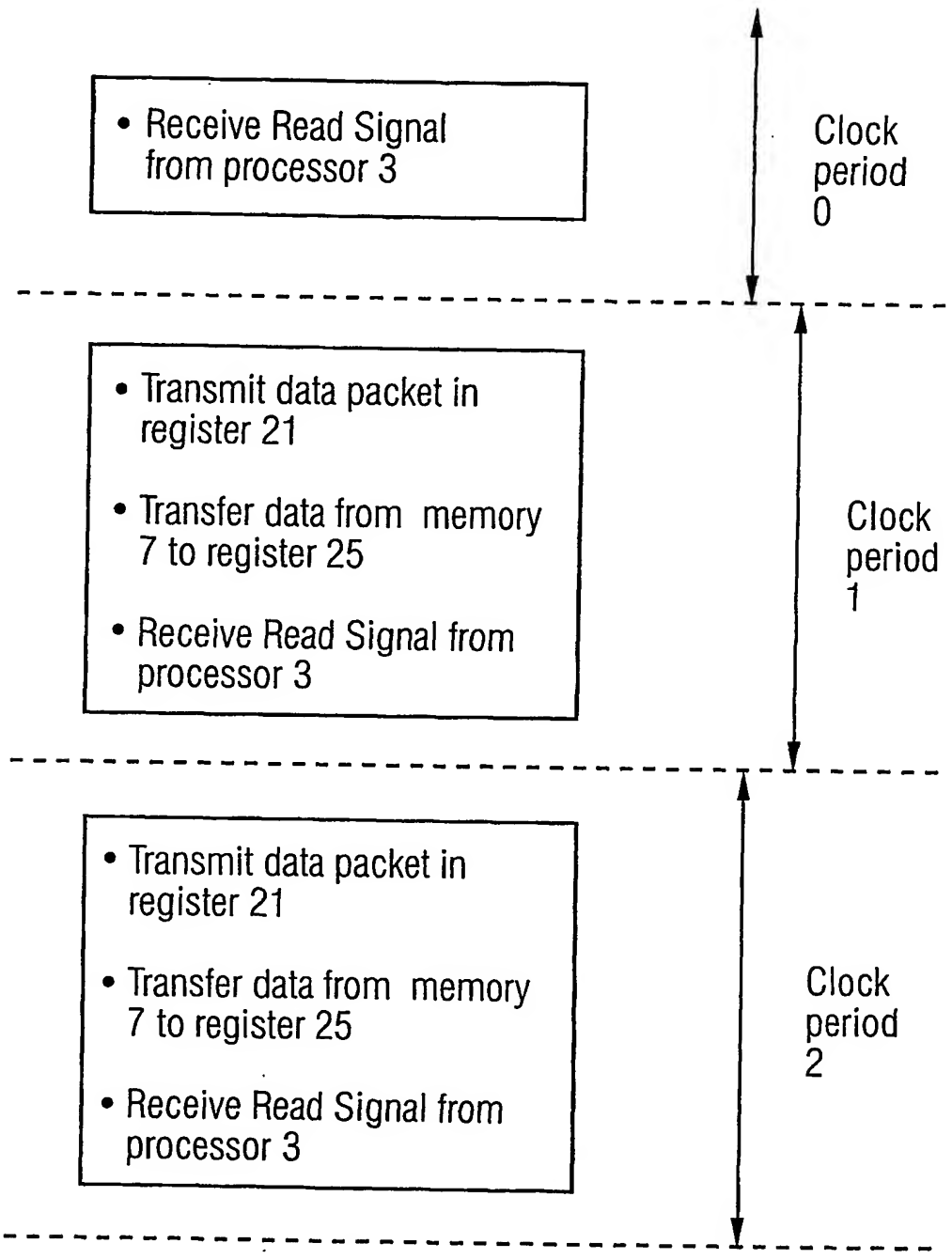


FIG 3


• Receive Read Signal from processor 3
Clock period 0
• Transmit data packet in register 21
• Transfer data from memory 7 to register 25
• Receive Read Signal from processor 3
Clock period 1
• Transmit data packet in register 21
• Transfer data from memory 7 to register 25
• Receive Read Signal from processor 3
Clock period 2

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 02/00270

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F15/167

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, IBM-TDB, INSPEC, EPO-Internal, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 640 929 A (ADVANCED MICRO DEVICES INC) 1 March 1995 (1995-03-01) abstract figure 2 column 4, line 1 -column 5, line 31	1-8
A	EP 0 376 003 A (IBM) 4 July 1990 (1990-07-04) abstract figures 1,2	1-8

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Sadoune, M-M

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